Design Verification Report

How the instrument works, and how the design was checked before hardware was built



Document	ZA1-DVR-012
Hardware revision	EVT-1 Rev B (including ECO-5)
Date	26 September 2026
Scope	Schematics, circuit simulation, PCB rule checks, power and thermal budget, FPGA, firmware and PC software, mechanics

1. Summary

The ZA-1 is a bench instrument that measures the **impedance** of electronic components (resistors, capacitors, inductors, sensors, cables, batteries, materials) from 20 Hz to 1 MHz. From one measurement it reports capacitance, inductance, resistance, loss (D), quality factor (Q) and phase, and it can sweep frequency and plot the results on its 7-inch screen. It follows the same measurement method (auto-balancing bridge, four-terminal-pair connection) as laboratory LCR meters that list at about USD 9,000–15,000 (list prices checked November 2026), built from current, readily available parts. The ZA-1 has not yet been built or measured against those instruments; every result in this report comes from simulation and rule checks.

Before any parts are bought, every part of the design was checked by simulation and by automated rule checks. The analog circuits were simulated directly from the schematic netlist, so what was simulated is exactly what will be built. The checks found **six real design problems**. All six are fixed in this revision (ECO-5), and the fixes were re-verified with the same simulations.

How to read the results. PASS (design check) means the design passed in simulation, in an automated rule check or in a software test. Nothing in this report was measured on a built instrument.

Area	What was checked	Result
Schematics (4 boards)	Electrical rules: unconnected pins, single-pin nets, undriven inputs, power pins; pin-by-pin review of every IC against its datasheet pin-out	**PASS (DESIGN CHECK)**
PCB layouts (4 boards)	KiCad design-rule check (clearances, drills, zones), every connection routed	**PASS (DESIGN CHECK)** 0 errors, 0 unrouted
Signal source	Output level, flatness, DAC image rejection	**PASS (DESIGN CHECK)** image -87 dBc
Measurement bridge	Stability of the balancing loop: 4 ranges × 5 cable lengths × 11 test parts (220 cases)	**FIXED** was oscillating with 1–2 m cables
Current channel	Does the current sensing load the range resistor?	**FIXED** 2 errors up to 50×
Accuracy	Error after calibration with ±5 °C drift of every component	**PASS (DESIGN CHECK)** ≤ 0.013 % at 1 kHz
Noise	Repeatability from all resistor and amplifier noise	**PASS (DESIGN CHECK)** ≤ 3 ppm (target 100)
Headroom	Every amplifier and ADC input, all parts 1 Ω – 10 MΩ, 20 Hz – 1 MHz	**PASS (DESIGN CHECK)** ≤ 60 % of limit
ADC drive	Settling of the ADC input between samples	**PASS (DESIGN CHECK)** ≤ 5.1 ppm
ADC reference	Stability of the reference buffer with 30 µF load	**FIXED** was at 3–9° margin
Input protection	Charged capacitor connected to the terminals	**FIXED** now survives 100 µF at 50 V
Power & thermal	Rail currents, regulator heat, mains fuse vs. switch-on surge, case temperature	**FIXED** fuse rating raised
Digital	SPI/QSPI/I²C signal quality and timing; FPGA logic simulation and 48 MHz timing	**PASS (DESIGN CHECK)** FPGA 51.7 MHz
Software	390 firmware checks, 74 PC-software tests, 82 FPGA checks	**PASS (DESIGN CHECK)**
Mechanics	3D collision check of all printed parts with the four populated boards	**PASS (DESIGN CHECK)** 0 collisions

In short: with ECO-5 applied, no simulation or rule check shows a problem that would stop the first prototype from working. What simulation cannot prove — real component tolerances, layout parasitics, and electromagnetic compatibility — is listed in section 6 together with the bench tests that close each item.

2. How it works

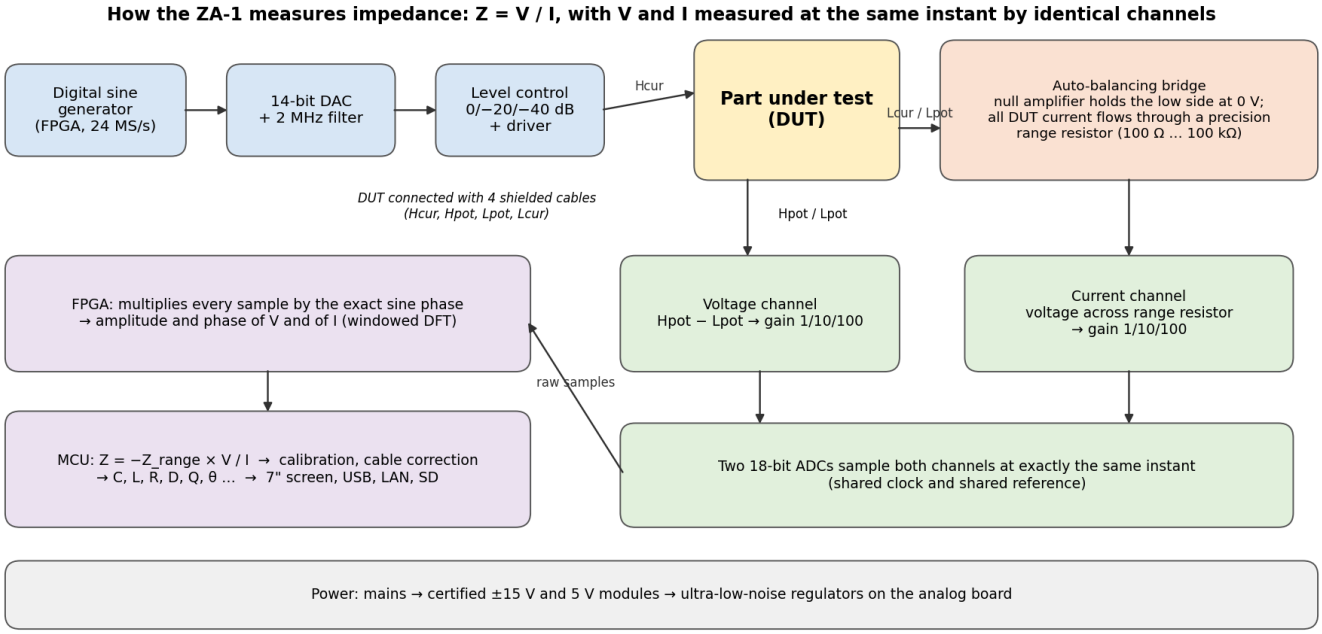


Figure 1. Block diagram of the instrument. The analog front end (top) generates the test signal and measures voltage and current; the main board (bottom left) controls everything and talks to the outside world.

The principle in one sentence

Impedance is voltage divided by current (Z = V / I). The ZA-1 applies a clean sine wave to the part, measures the voltage across it and the current through it *at exactly the same instant*, and divides one by the other. Because both measurements go through identical circuits and are digitised by two identical converters that share a clock and a reference, most error sources are the same in both and cancel in the division.

Step by step

1. **Sine generator.** The FPGA computes a sine wave 24 million times per second with a frequency resolution of 0.006 Hz. A 14-bit digital-to-analog converter turns it into a voltage, and a filter removes the digital steps. Relays add −20 dB or −40 dB of attenuation for low test levels.
2. **Four-terminal connection.** The part is connected with four shielded cables. Two carry the test current (Hcur, Lcur); the other two only sense voltage (Hpot, Lpot), so the resistance of cables and contacts does not enter the measurement. This is the connection standard of professional LCR meters, and the ZA-1 uses the same 22 mm BNC spacing, so existing fixtures plug straight in.
3. **Auto-balancing bridge.** A fast amplifier (the "null amplifier") holds the low side of the part at exactly 0 V by pulling the part's current through a precision range resistor (100 Ω, 1 kΩ, 10 kΩ or 100 kΩ). The voltage across that resistor is therefore a precise copy of the current.
4. **Two matched channels.** The voltage channel measures Hpot − Lpot; the current channel measures the voltage across the range resistor. Each has a switchable gain of 1, 10 or 100, chosen automatically so the signals use most of the converter range.
5. **Simultaneous 18-bit sampling.** Two AD4003 converters sample both channels on the same clock edge.
6. **Digital demodulation.** The FPGA multiplies every sample by the exact sine phase used to generate the signal and sums the products (a windowed discrete Fourier transform). This extracts amplitude and phase of V and I at the test frequency and rejects noise and harmonics.
7. **Calculation and correction.** The microcontroller divides V by I, applies the factory calibration and the user's OPEN/SHORT/LOAD cable correction, and converts the result into C, L, R, D, Q and phase for the display, USB, network and SD card.

The four boards

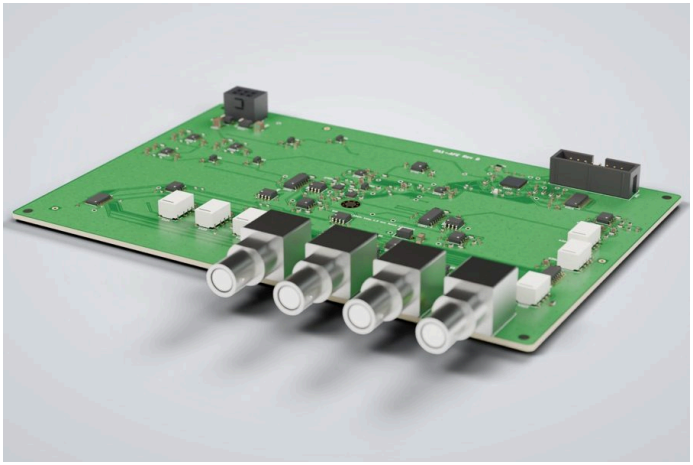


Figure 2. **Analog front end (AFE)** — sine source, bridge, the two measurement channels, ADCs, FPGA. 4-layer.

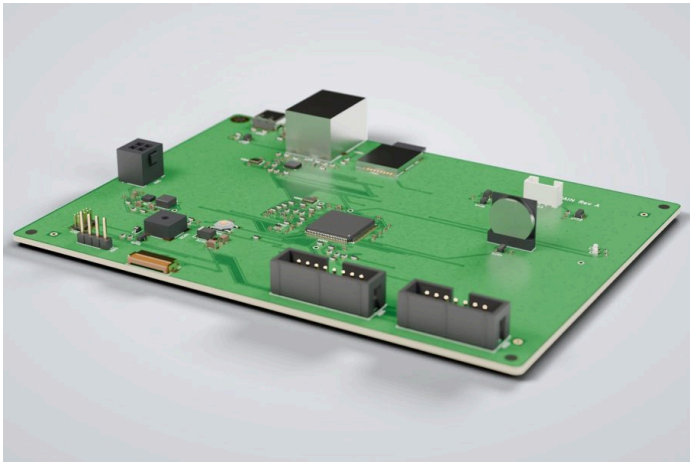


Figure 4. **Main board** — 480 MHz microcontroller, display interface, USB, Ethernet, SD card, trigger I/O. 4-layer.

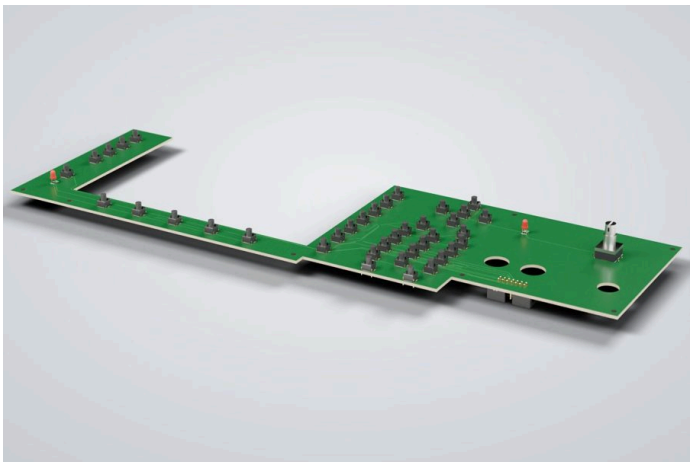


Figure 3. **Front panel** — 37 keys, rotary knob, indicators. 2-layer.

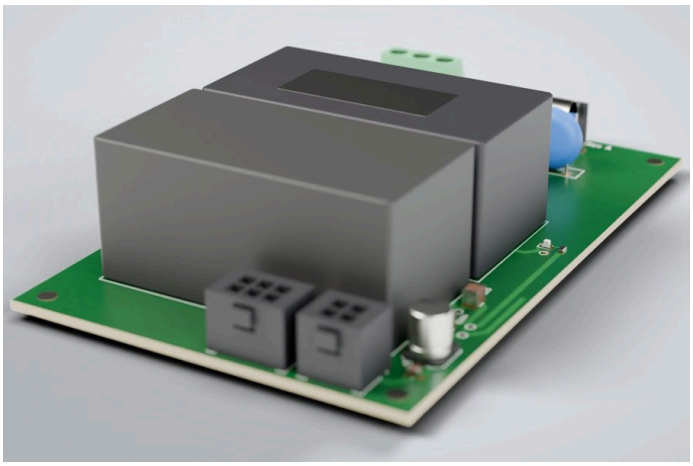


Figure 5. **Power supply** — mains filter and two certified AC/DC modules (±15 V analog, 5 V digital). 2-layer.

3. How the design was checked

Each check answers one question an engineer would ask before paying for boards: *will it power up, will it be stable, will it be accurate, will it survive normal mistakes, and does every connection exist?*

Circuit simulation straight from the schematic

A converter program reads the netlist exported from the KiCad schematic and writes a SPICE circuit for the whole analog signal path — source, bridge, both channels, ADC drivers and reference (about 300 components). Every resistor and capacitor value, every amplifier and every relay contact comes from the schematic, so a wrong value or a wrong connection in the schematic shows up in the simulation. Relays and gain switches are set per test case, exactly as the firmware sets them. The simulations ran in ngspice 42.

Integrated circuits are represented by models built from their datasheet figures: gain, bandwidth, second pole, slew rate, output resistance, input capacitance, noise, supply current and output swing. The test cables are modelled as real transmission lines, because their resonances are what makes the measurement loop hard to stabilise. Where a datasheet figure is not published (for example an amplifier's open-loop output resistance), the check is repeated over a range of values and the design must pass for all of them.

Rule checks and software tests

- **Electrical rules** on the netlist of all four boards, plus a pin-by-pin table of every IC that was compared with the datasheet pin-out.
- **PCB design-rule check** (KiCad) with all copper zones re-filled, on all four boards.
- **FPGA**: cycle-accurate logic simulation against a bit-exact reference model, and place-and-route timing analysis at the 48 MHz clock.
- **Firmware**: the complete measurement engine, calibration, SCPI remote control and user interface run on a PC against a simulated analog board.
- **PC software**: unit and integration tests, including tests against the firmware simulator.
- **Mechanics**: solid-body collision check of every printed part with the four populated board models.

4. Problems found and fixed (ECO-5)

These are the problems the verification found. Each was fixed in the schematic, the PCB, the firmware or the documentation, and re-checked with the same simulation that found it.

#	Problem found	Why it mattered	Fix	Proof after the fix
1	The current channel's 1 kΩ input resistors were connected straight across the range resistor.	The effective range resistor became Rr ‖ 2 kΩ: errors of 5 %, 50 %, 500 % and 5 000 % on the four ranges, and the 10 k/100 k ranges lost almost all their signal.	Two unity-gain FET buffers (THS4631) on the Kelvin taps, like the voltage channel already had.	Before calibration ≤ 0.2 % at 1 kHz on every range; after calibration ≤ 0.01 % (section 5.3).
2	A 1 MΩ bias resistor sat across the range resistor.	1 % error on the 100 kΩ range, drifting with the resistor's temperature coefficient.	Bias resistors moved to ground, where they carry no measurement current.	As above.
3	The bridge loop oscillated with 1–2 m test cables.	Rail-to-rail oscillation in the time-domain simulation (section 5.2): measurements would be impossible with normal fixtures.	1 kΩ + 15 pF local compensation, 47 Ω output isolation, 470/220 pF range capacitors, RC terminations on the Lpot and Lcur inputs; firmware uses the new range impedance.	Phase margin ≥ 49° for 0–2 m and ≥ 39° at 4 m in all 220 cases; clean step response.
4	The ADC reference buffer drove 30 µF directly.	Phase margin 3–9°: likely to ring or oscillate, adding noise to every reading.	1 Ω isolation resistor (the 0 Ω placeholder already on the board).	Phase margin 89° for every assumed amplifier output resistance.
5	Clamp diodes sat directly on the Hcur and Lcur terminals.	A charged 100 µF capacitor at 30–50 V would push 1.5–8 A through diodes rated 1 A, and pump the ±12 V rails.	Hcur clamp moved behind the 100 Ω source resistor; 22 Ω surge resistor before the Lcur clamp; both anti-surge types.	≤ 0.2 A for 100 µF at 50 V (125 mJ), within rating.
6	Mains fuse T1 A.	The two power modules' switch-on surge used 45 % of the fuse's I²t: nuisance blowing over time.	Inlet fuses T2 A; board fuse T3.15 A (the module maker's recommendation).	Surge now 9 % / 3 % of fuse I²t.
–	PCB rule check: 2 clearance markers at the Kelvin net-tie and 1 incomplete thermal relief (FRONT).	Would stop a board house's automatic check.	Tracks re-routed at the net-tie, thermal made solid.	0 DRC errors on all boards.

Also updated with ECO-5: bill of materials, fabrication files, 3D models, renders, the printed rear-panel label (fuse rating), the power budget (12 amplifiers instead of 10), the user manual (protection limits, cable lengths) and the theory-of-operation document.

5. Results in detail

5.1 Signal source

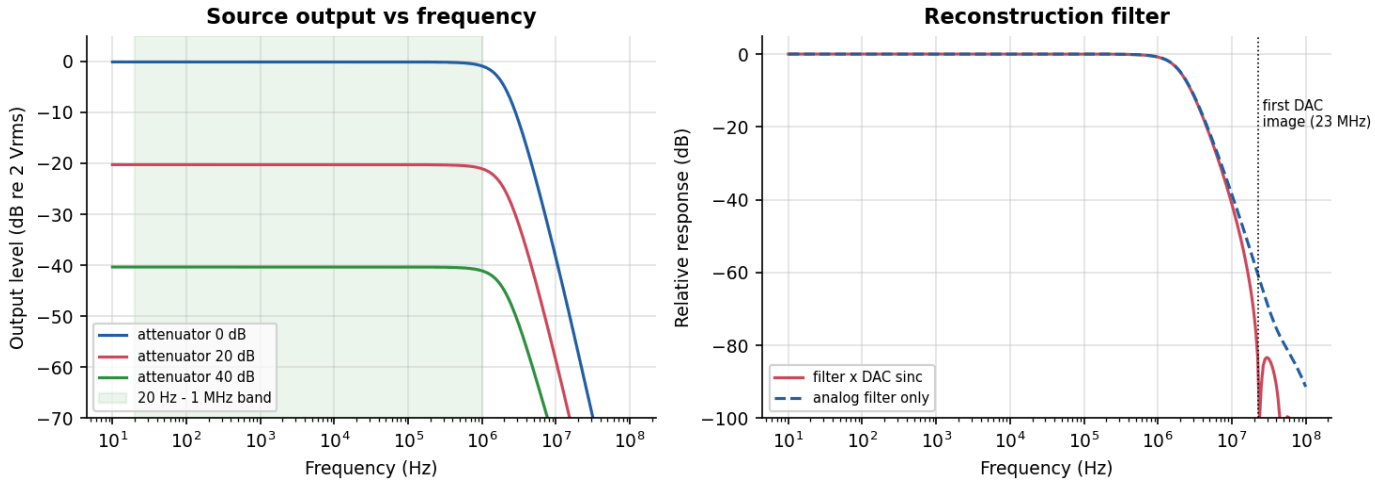


Figure 6. Left: source output level for the three attenuator settings. Right: the reconstruction filter together with the DAC's own sin(x)/x roll-off.

The output is flat across the measurement band and drops only -0.8 dB at 1 MHz (the level control loop compensates this). The attenuator gives −20.2 dB and −40.2 dB. The first digital image at 23 MHz is suppressed by 87 dB, so the ADCs see a clean sine. Full-scale output: 1.97 Vrms. Result: **PASS (DESIGN CHECK)**

5.2 Stability of the measurement bridge

The null amplifier, the range resistor, the test cables and the part under test form a feedback loop. If that loop has too little phase margin, it rings or oscillates. The loop was analysed with a general loop-gain method (Middlebrook voltage and current injection) at the point where the Lpot cable enters the board, for every combination of range (4), cable length (0, 0.5, 1, 2, 4 m) and test part (open, short, 10 Ω, 1 kΩ, 100 kΩ, 10 pF, 100 pF, 10 nF, 1 µF, 100 µH, 10 mH).

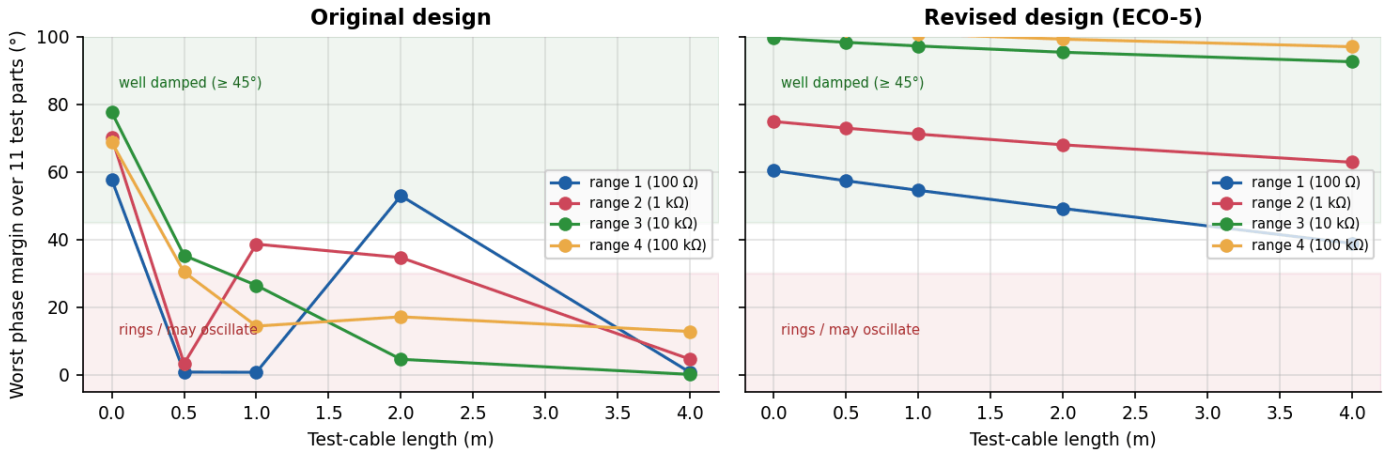


Figure 7. Worst-case phase margin of the bridge loop versus cable length. Left: original design. Right: after ECO-5.

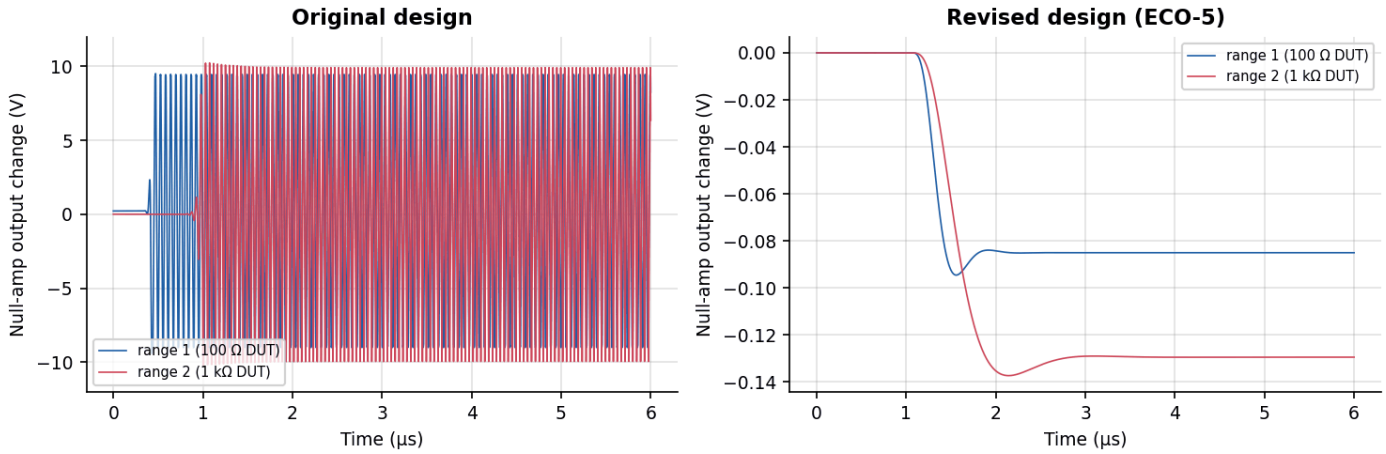


Figure 8. Time-domain check with 2 m cables: response of the null amplifier to a small step of the test signal.

The original design had almost no phase margin once real cables were connected and oscillated from rail to rail (18 V peak-to-peak) in the time-domain simulation. After ECO-5 the worst phase margin is 49° with cables up to 2 m and 39° with 4 m cables, and the peak closed-loop sensitivity is 2.7 dB (≤ 2 m). The loop settles cleanly. Result: **FIXED → PASS (DESIGN CHECK)**

5.3 Accuracy

Each range was calibrated in the simulation the way the factory will do it (OPEN, SHORT and a reference resistor through a 1 m cable). Then every resistor and capacitor in the signal path was shifted by its temperature coefficient for a +5 °C change (random direction, six random draws), the amplifier bandwidth was reduced by 1 %, and the relay contact resistance was raised by 50 mΩ. Resistors, capacitors and inductors spanning each range were then measured.

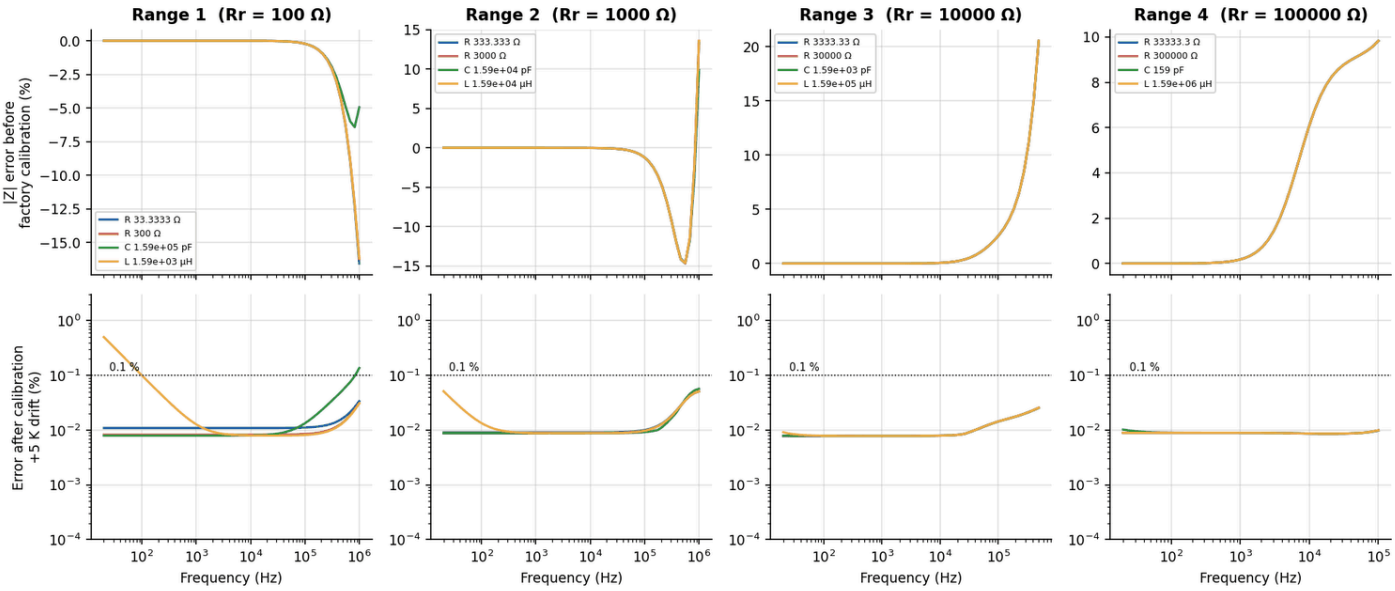


Figure 9. Top: error before factory calibration (with the firmware's nominal range model). Bottom: worst error after calibration once the instrument has drifted by 5 °C.

Before calibration the error is essentially zero at low frequency and grows to 10–20 % at the top of each range's band (limited bridge gain and cable effects). These errors are stable and linear, so calibration removes them: after calibration plus drift, the worst error is 0.013 % at 1 kHz, 0.015 % at 100 kHz and 0.14 % at the top frequency — inside the ±0.1 % basic-accuracy target. Calibration-standard uncertainty and fixture technique add to this (error budget, doc 04). Result: **PASS (DESIGN CHECK)**

5.4 Noise and repeatability

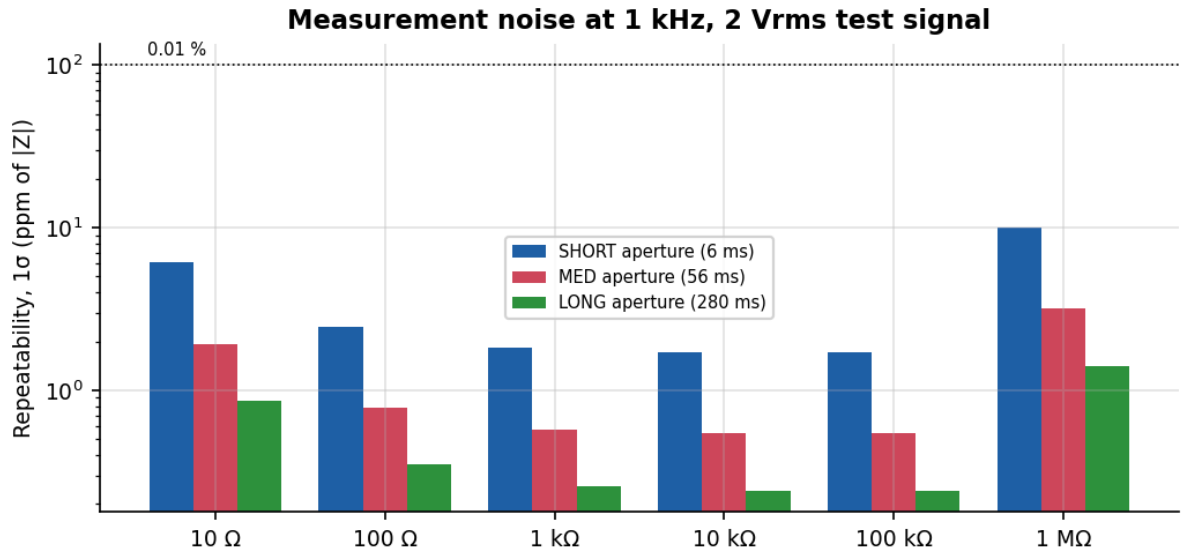


Figure 10. Expected scatter of repeated readings (1 sigma) from all thermal and amplifier noise, 1 kHz, 2 Vrms.

Noise analysis over the full circuit (every resistor and amplifier) plus the ADC's own noise gives a repeatability of 0.5–3.2 ppm (0.0001–0.0003 %) at the standard measurement speed — far better than the 100 ppm specification. In practice, low-frequency (1/f) noise, mains pickup and the test fixture will dominate. Result: **PASS (DESIGN CHECK)**

5.5 Signal headroom

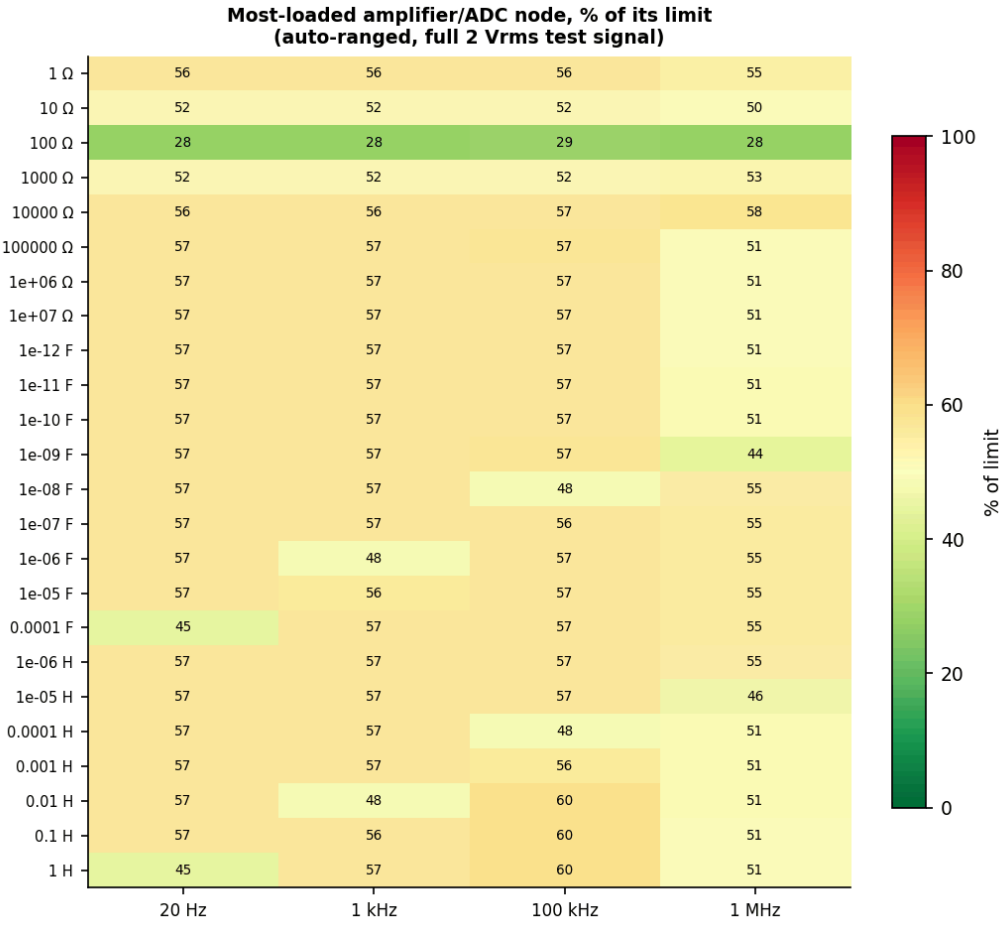


Figure 11. Largest signal on any amplifier output or ADC input, as a percentage of what that node can handle, with the automatic range selection the firmware uses.

For 96 combinations of part and frequency — from 1 Ω to 10 MΩ, 1 pF to 100 µF and 1 µH to 1 H — no node exceeds 60 % of its limit at the full 2 Vrms test level. Nothing clips. Result: **PASS (DESIGN CHECK)**

5.6 ADC input settling

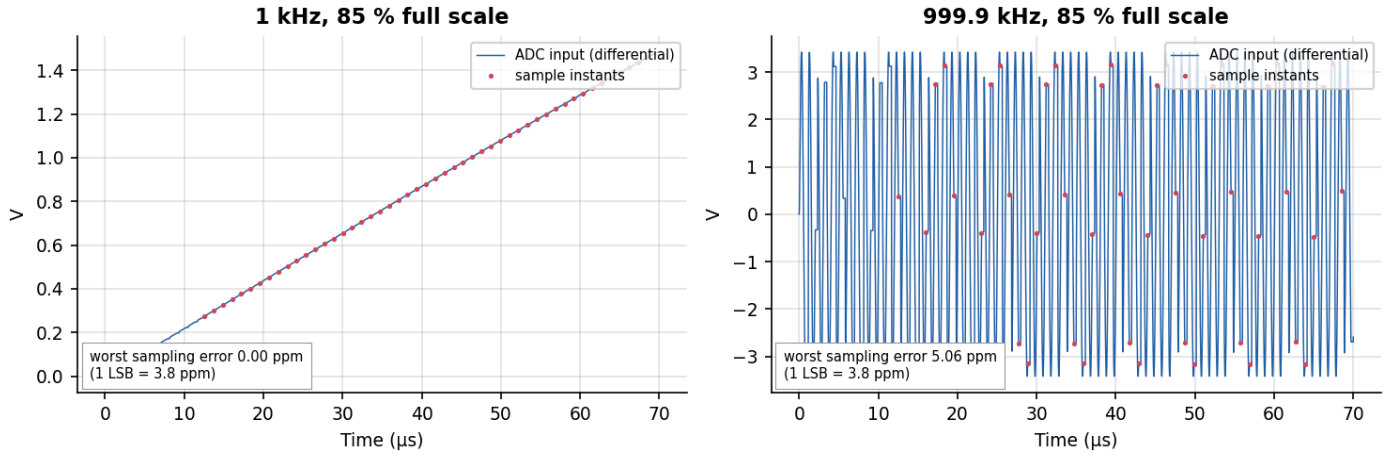


Figure 12. Each AD4003 converter briefly connects a 40 pF sampling capacitor to its driver. The error is the difference between the sampled value with the real switching input and with an ideal one.

The ADC driver and its RC filter settle to 0.002 ppm at 1 kHz and 5.1 ppm at 1 MHz full scale (one 18-bit step is 3.8 ppm). Both channels see the same effect, so it largely cancels in V/I. Result: **PASS (DESIGN CHECK)**

5.7 ADC reference

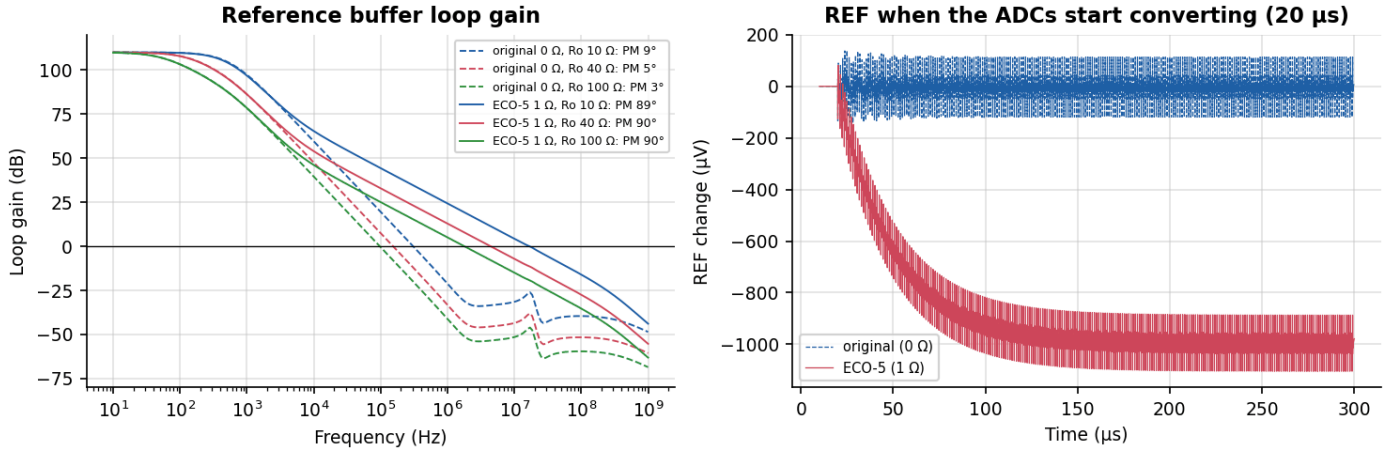


Figure 13. Left: loop gain of the reference buffer (dashed: original 0 Ω, solid: ECO-5 1 Ω). Right: reference voltage when the converters start sampling.

Driving 30 µF directly, the buffer had only 3–9° of phase margin. With a 1 Ω isolation resistor it has ≥ 89°. The resistor causes a constant 1 mV drop that both converters share, so it cancels in V/I. Result: **FIXED → PASS (DESIGN CHECK)**

5.8 Charged-capacitor protection

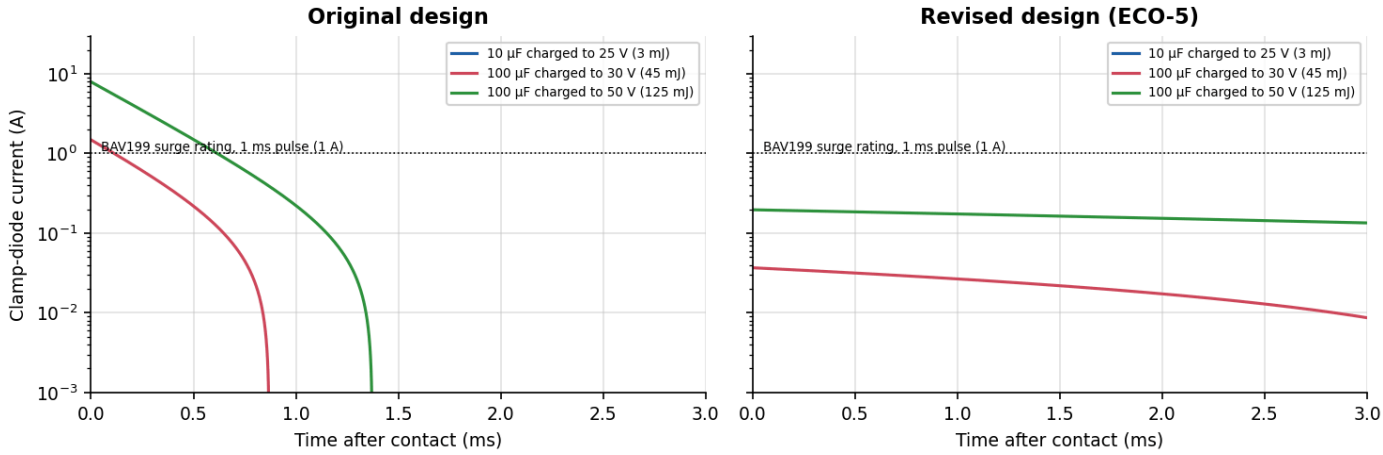


Figure 14. Current into the protection diodes when a charged capacitor touches the terminals (piece-wise model of the protection path).

Connecting a charged capacitor is the most common way LCR meters are damaged. In the original design a 100 µF capacitor at 50 V drove 7.9 A into diodes rated 1 A. With the diodes moved behind 100 Ω and 22 Ω surge resistors, the peak is 0.20 A. The instrument is rated for charged capacitors up to 42 V (the terminal voltage rating) with margin to 50 V / 125 mJ; the user manual tells users to discharge capacitors first. Result: **FIXED → PASS (DESIGN CHECK)**

5.9 Power, heat and mains fuse

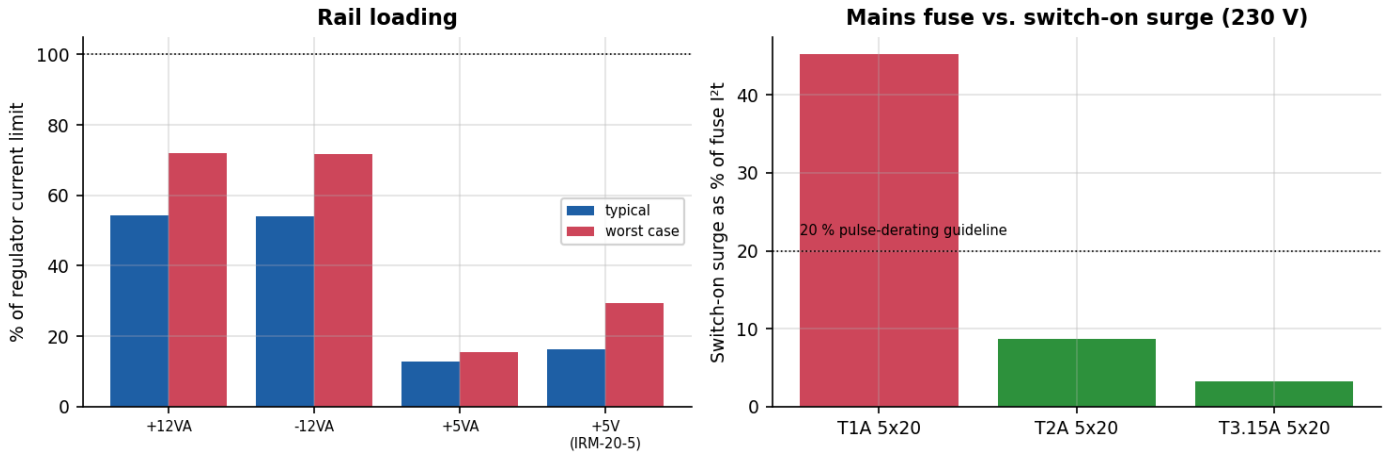


Figure 15. Left: current on each supply rail as a share of its regulator limit. Right: switch-on surge of the two power modules as a share of the fuse I²t rating.

Every rail runs at ≤ 72 % of its limit in the worst case. The low-noise regulators dissipate at most 0.65 W each (junction +26 °C). The instrument draws about 10 W typical and 16 W worst case from the mains; inside the closed case the air warms by about 8 °C, well within the printed ASA enclosure's limits. The combined switch-on surge of the two power modules (1.2 A²s) was 45 % of a T1 A fuse's rating; the fuses were raised to T2 A (inlet) and T3.15 A (board). Result: **FIXED → PASS (DESIGN CHECK)**

5.10 Mains filter

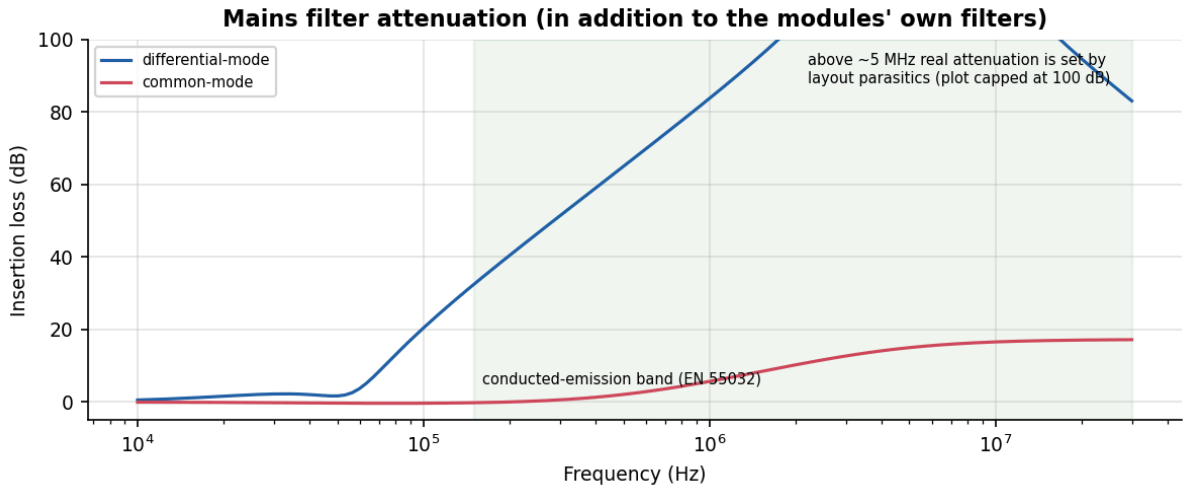


Figure 16. Attenuation of the mains filter on the power-supply board for differential and common-mode noise.

Both power modules are certified to EN 55032 class B on their own. The ZA-1 itself has not yet been tested or certified to any EMC, safety or radio standard. The board filter adds 32 dB of differential-mode attenuation at 150 kHz and more above. Common-mode attenuation is modest (no Y-capacitors, to keep earth leakage near zero); an EMC pre-scan is on the bench-test list. Result: **PASS (DESIGN CHECK) / NOTE**

5.11 Board-to-board signals

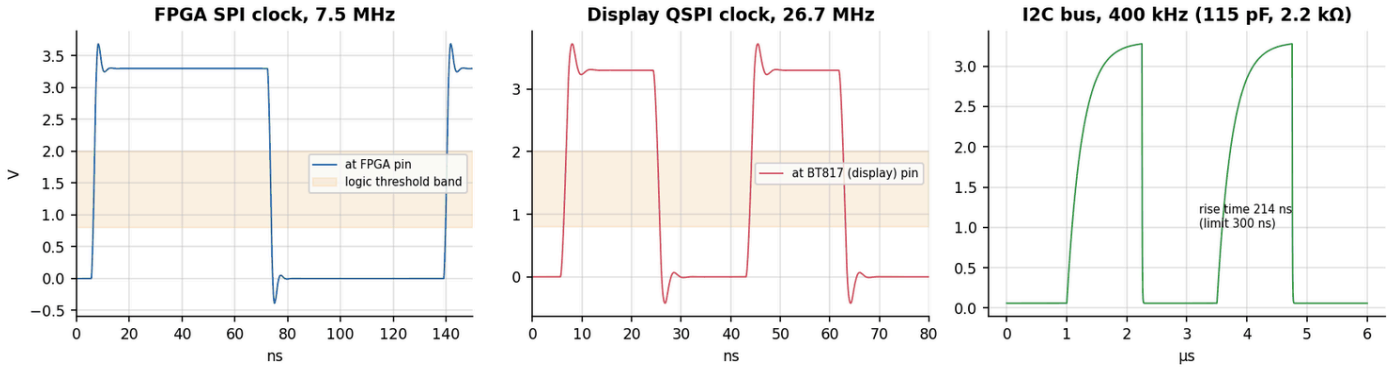


Figure 17. Clock waveforms at the receiving pins, including ribbon/flat-flex cables and series resistors; I²C bus rise time with the pull-ups and total bus capacitance.

The FPGA SPI clock (7.5 MHz over the 70 mm ribbon) and the display QSPI clock (26.7 MHz over the flat-flex cable) switch cleanly with ≤ 0.4 V overshoot and no re-crossing of the logic threshold. The shared I²C bus rises in 214 ns against a 300 ns limit at 400 kHz. Result: **PASS (DESIGN CHECK)**

5.12 FPGA, firmware and PC software

Item	Check	Result
FPGA logic	82 register checks + 8 closed-loop measurement simulations (20 Hz – 1 MHz, undersampling, rectangular window), bit-exact against the reference model	**PASS (DESIGN CHECK)** error ≤ $4 \cdot 10^{-5}$, ≤ 0.005°
FPGA timing	Place and route on iCE40UP5K, 48 MHz system clock	**PASS (DESIGN CHECK)** 51.7 MHz (8 % margin)
Firmware	390 checks: DSP, ranging, calibration, accuracy, SCPI, sweeps, user interface, safety, settings	**PASS (DESIGN CHECK)** 0 failures
Firmware build	ARM Cortex-M7 image (updated for ECO-5)	**PASS (DESIGN CHECK)** 305 kB flash
PC software	74 tests incl. tests against the firmware simulator	**PASS (DESIGN CHECK)** 0 failures

5.13 Schematic and PCB rule checks

Board	Parts	Nets	ERC issues	Layers	Unrouted	DRC errors	Silk warnings	Result
ZA1-AFE	328	247	0	4	0	0	12	**PASS (DESIGN CHECK)**
ZA1-MAIN	141	144	0	4	0	0	2	**PASS (DESIGN CHECK)**
ZA1-FRONT	73	54	0	2	0	0	0	**PASS (DESIGN CHECK)**
ZA1-PSU	26	12	0	2	0	0	0	**PASS (DESIGN CHECK)**

DRC warnings not counted as errors: "footprint not found in library" (the footprints are embedded in the board files; the warning only means the KiCad libraries are not installed on the checking machine) and silkscreen lines clipped at the board edge (cosmetic, the board house trims them). Unconnected IC pins were reviewed one by one: they are spare FPGA/MCU I/O, unused display-connector pins, and open-drain "power good" outputs that the design does not use.

6. What simulation cannot prove, and how the prototype closes it

Simulation shows that the design is correct on paper and robust to the variations that were modelled. The following can only be settled on real hardware. Each has a planned bench test (doc 05, Test & Calibration).

Item	Why it is open	How it is closed
Real amplifier behaviour at 10–200 MHz	Datasheet models, not the vendors' full SPICE models (not downloadable from the build environment).	Bring-up: inject a step, check the null-amplifier output with 0/1/2/4 m cables; re-run the loop-gain script with the vendor models.
PCB parasitics	Copper traces add capacitance and inductance not in the schematic.	Hand review of the AFE layout (guard rings around LPOT_N, short Kelvin traces); first-article measurements.
Absolute accuracy	Depends on the calibration standards and fixtures.	Factory calibration with traceable 4TP standards; compare against a reference LCR meter (doc 04).
EMC	Radiated and conducted emissions and immunity need a test lab.	Pre-compliance scan (EN 61326-1) on the first prototype.
Datasheet details to confirm	Omron G6K coil polarity (pin 1 = +); Riverdi 7" display timing; IEC inlet cut-out; trigger-jack part numbers; shield-can flat pattern.	Check against the purchased parts before ordering the full set.

Recommended next steps

1. Order 3 EVT sets of the four boards and print one enclosure.
2. Power up board by board with a current-limited supply; check rails, then the bridge with 1 m and 2 m cables.
3. Run factory calibration with 4TP standards and compare 5 frequencies × 7 standards against a reference instrument.
4. EMC pre-scan; then design-validation build.

Appendix A — Models and tools

Part	Model parameters used (from the manufacturer's datasheet)
TI THS4631 (12 used)	open-loop gain 72 dB, gain-bandwidth 210 MHz, 2nd pole 450 MHz, slew rate 1000 V/µs, 7 nV/√Hz, input 3.9 pF, output resistance 12 Ω, supply 12.5 mA
ADI ADA4940-1 (2)	fully differential, 90 dB, 200 MHz, 95 V/µs, 3.9 nV/√Hz, output swing 0.1–4.9 V on 5 V
ADI ADA4807-1 (reference buffer)	110 dB, 180 MHz, 225 V/µs, 3.1 nV/√Hz, open-loop output resistance swept 10–100 Ω
ADI AD4003 (2)	400 Ω / 40 pF switched sampling input, 290 ns conversion, SNR 100.5 dB
Vishay DG412, Omron G6K	25 Ω on-resistance, 5–17 pF switch capacitance; relay contact 50 mΩ, 1 pF open
Nexperia BAV199	IS 5 pA, n 1.9, RS 1.5 Ω, CJ 1.5 pF
Test cables	50 Ω coax transmission lines, 5 ns/m, shields joined at the part (4TP rule)
Mains filter	10 mH common-mode choke with 1.2 % leakage and 4.7 kΩ core loss, X2 capacitors with 12 nH ESL

Tools: KiCad 7 (schematics, PCB, DRC), ngspice 42 (circuit simulation), Python (netlist-to-SPICE converter, analysis, plots), Icarus Verilog + Yosys + nextpnr (FPGA), GCC (firmware), pytest (PC software), CadQuery/OpenCASCADE (mechanics). All scripts and raw results are in the `07_Verification` folder of the design package, so every result in this report can be regenerated.