ZA-1 Precision Impedance Analyzer — System Specification

Document: ZA1-SPEC-001 Rev A (2026-09-25) Status: Design baseline for EVT-1 (first engineering build)

1. Product summary

The ZA-1 is a benchtop precision LCR meter / impedance analyzer, 20 Hz – 1 MHz, using the same **auto-balancing bridge (ABB)** measurement principle as the Keysight E4980A. It has an E4980A-style front panel (ECO-4): 7" 1024×600 display with 6 softkeys, full keypad, navigation cross and knob, a GRAPH mode, four BNC 4-terminal-pair (4TP) UNKNOWN terminals plus TRIG IN/OUT and a GND post on the front, and USB-TMC, LAN (SCPI raw socket) and microSD on the rear. The case is 3D-printed (400 × 135 mm).

Benchmark reference: Keysight E4980A (20 Hz–2 MHz, 0.05 % basic accuracy). The ZA-1 targets **0.1 % basic accuracy** over a narrower range. It is a realistic EVT-1 target for this architecture after the full calibration in doc 05. The E4980A's 0.05 % comes from decades of refinement and factory calibration against traceable standards. The ZA-1 can approach it only with the same discipline (see 04_Error_Budget.pdf).

2. Performance targets (EVT-1 design goals, to be verified in DVT)

Parameter	Target
Frequency range	20 Hz – 1 MHz, 0.01 Hz resolution (NCO 32-bit @ 24 MSPS → 5.6 mHz)
Frequency accuracy	±0.005 % (48 MHz reference, ±25 ppm XO; TCXO option ±2.5 ppm)
Test signal level	5 mVrms – 2.0 Vrms open-circuit (2.03 Vrms full scale), 1 mV resolution; 0 dB / −20 dB / −40 dB attenuator
Level accuracy	±(5 % + 1 mV) uncorrected; ±1 % with ALC (firmware constant-voltage loop)
Source impedance	100 Ω ±1 %
Measurement ranges	100 Ω, 1 kΩ, 10 kΩ, 100 kΩ range resistors × PGA gain 1/10/100 on both channels; auto / hold
Displayed	Z
Basic accuracy	±0.1 %
Repeatability	0.01 % (1 σ, same conditions)
Measurement time	SHORT ≈ 6 ms, MED ≈ 60 ms, LONG ≈ 300 ms (f ≥ 1 kHz); minimum 8 signal cycles
Parameters	Cp-D, Cp-Q, Cp-G, Cp-Rp, Cs-D, Cs-Q, Cs-Rs, Lp-D, Lp-Q, Lp-G, Lp-Rp, Ls-D, Ls-Q, Ls-Rs, R-X, Z-θd, Z-θr, G-B, Y-θd, Y-θr
Sweep	2–1601 points, lin/log frequency or level; Bode / Nyquist plots on screen and in host app
Correction	OPEN, SHORT, LOAD (spot + multi-point), cable length 0/1/2 m (bridge loop verified stable with 0–4 m 4TP cables)
Comparator / bin sort	10 bins + OUT, pass/fail beeper (Handler I/O is a future option)
Interfaces	USB-C (USB-TMC, USB488), 10/100 Ethernet (SCPI port 5025, LXI-style discovery), microSD, TRIG IN / TRIG OUT BNC (3.3 V LVTTL, 5 V tolerant input)

Parameter	Target
Display / UI	7.0" 1024×600 IPS (Riverdi RVT70HSBNWN00, BT817Q EVE4); 37 keys + power key (softkeys, menu keys, numeric keypad, navigation cross) + push encoder; GRAPH page (|Z|/θ, R-X, Cs-D, Ls-Q, Nyquist)
Power	100–240 VAC, 50/60 Hz, ≤ 25 W; IEC C14 inlet with 2 × T2 A fuses and switch
Warm-up	30 min to full accuracy
Environment	0–40 °C operating, full spec 23 ± 5 °C, ≤ 80 % RH non-condensing
Dimensions	400 W × 135 H × ≈ 250 D mm (excl. feet and handle); ≈ 2.5 kg (3D-printed enclosure, ECO-4c)
Input protection	Discharge DUT capacitors first. Rated for a charged capacitor up to 42 V / 100 µF connected to UNKNOWN; protection verified to 50 V / 125 mJ (ECO-5, verify report §5.8)
Safety / EMC intent	IEC 61010-1 (Measurement category: none, UNKNOWN terminals are not mains-rated), EN 61326-1 class B. Certified AC/DC modules are used so the mains side stays inside pre-approved parts

3. Architecture

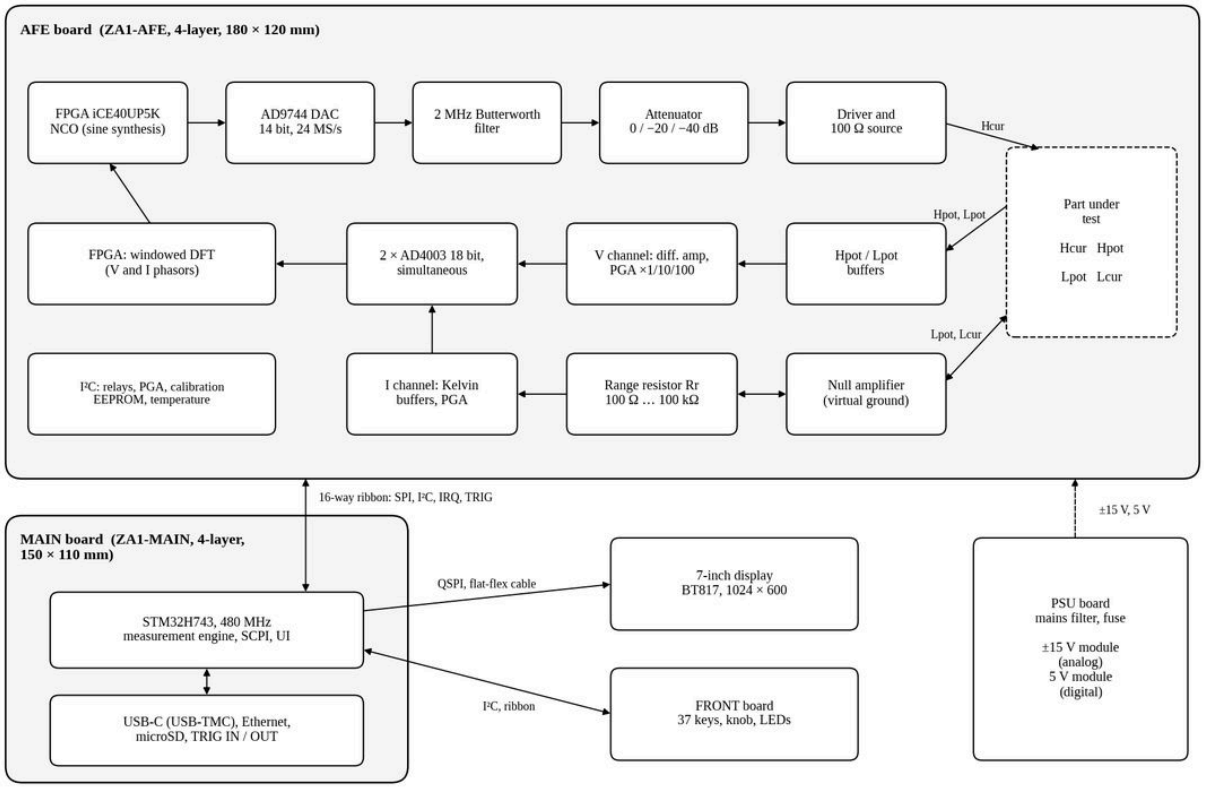


Figure 1. ZA-1 system block diagram.

The AFE board carries the whole analog signal path. The FPGA synthesises the test sine (32-bit NCO) and drives the AD9744 DAC; the output is filtered (2 MHz Butterworth), attenuated by relays in 0, −20 or −40 dB steps and driven into the Hcur terminal through a 100 Ω source resistor. The Hpot and Lpot terminals are buffered by THS4631 followers and subtracted in a differential amplifier to give the voltage channel. The null amplifier holds Lpot at virtual ground so that the current through the part flows through the range resistor Rr (100 Ω, 1 kΩ, 10 kΩ or 100 kΩ, selected by G6K relays); a Kelvin tap across Rr, buffered by U604/U605, gives the current channel. Both channels pass a programmable gain stage (×1/10/100) and an ADA4940 driver into two AD4003 18-bit ADCs that share one convert signal. The

FPGA applies a Blackman-Harris window and computes the DFT at the test frequency, using the NCO phase at each sample instant as the reference. A TCA9555 expander switches relays and gains, a 24LC256 EEPROM holds the calibration and a TMP117 reports board temperature.

The MAIN board is built around an STM32H743 (480 MHz Cortex-M7). It is connected to the AFE by a 16-way ribbon (SPI, FPGA configuration, IRQ, trigger and I²C) and provides Ethernet (LAN8742A), USB-C (USB-TMC), microSD, the trigger input and output, the beeper and the 3.3 V supply. The 7-inch BT817 display is driven over QSPI through a 20-way flat-flex cable; the FRONT board (37 keys on three TCA9555 expanders, EC11 encoder, power key and indicators) is on a 14-way ribbon. The PSU board takes mains through the IEC inlet, fuse, MOV, X-capacitor and common-mode choke into two certified modules: a RECOM RAC20-15DK (±15 V, isolated) for the analog circuits and a MEAN WELL IRM-20-5 (5 V, 4 A) for the logic.

3.1 Why these choices

- **Auto-balancing bridge.** This is the standard method for 20 Hz–a few MHz (Keysight E4980A, 4284A). It gives a true virtual-ground Lpot node, so stray capacitance to guard does not load the DUT.
- **Direct digital synthesis and sampling on one clock.** The source NCO and the ADC sample clock both come from the same 48 MHz oscillator. The demodulation reference is the *exact* DDS phase at each conversion instant. Source phase noise and frequency error therefore cancel in the V/I ratio.
- **Simultaneous dual 18-bit SAR (AD4003, 2 MSPS rated).** V and I are sampled at the same instant, so there is no inter-channel timing skew. The SAR has no pipeline latency or 1/f droop at 20 Hz. Above fs/2 (≈ 430 kHz), the system uses *coherent bandpass undersampling*. The ADC's 10 MHz input bandwidth and the identical V/I paths make this valid, and firmware chooses fs so the alias lands near fs/4.
- **Windowed DFT (4-term Blackman–Harris).** Sidelobes are −92 dB. The −f image and harmonics cannot bias the fundamental, whether or not the record holds an integer number of cycles. Any window error is common to V and I and cancels in the ratio.
- **Kelvin-sensed range resistors.** The I-channel reads the voltage directly across Rr through the second relay pole, so relay contact resistance is outside the measurement.
- **Certified AC/DC modules.** Mains safety and EMC risk sit inside pre-certified parts. That matters for selling the product.

4. Board partition

Board	Doc/Project	Layers	Size (mm)	Function
ZA1-AFE	hardware/afe	4 (S-G-P-S)	180 × 120	Analog front end, DAC, ADCs, FPGA, relays, cal EEPROM
ZA1-MAIN	hardware/main	4 (S-G-P-S)	150 × 110	MCU, comms, display, storage, rear I/O
ZA1-FRONT	hardware/front	2	386 × 125 (U-shaped, Rev B)	Keypad (37 keys + power), encoder, LEDs
ZA1-PSU	hardware/psu	2 (2 oz)	70 × 110	Mains entry, AC/DC modules

5. Mechanical envelope (chassis coordinates) — ECO-4c (printed enclosure, front panel layout v3)

Source of truth: `docs/front_panel_layout.json` (v3, ECO-4c) and `mechanical/cad/za1_enclosure_print.py`. The sheet-metal envelope of Rev A + ECO-1..3 (240 × 110 × 280) is superseded.

Origin: X = 0 at the left **outer** face, Y = 0 at the **inner** face of the front panel (panel at −Y), Z = 0 at the **floor outer face**. +X to the right (viewed from the front), +Y toward the rear, +Z up. Units are mm.

- Chassis: 3D-printed ASA, **400 (X) × 135 (Z)**, 249.7 deep from the bezel front (Y −7.5) to the rear frame (Y 242.15); feet add 8 mm. Wrap-around front bezel Y −7.5 … 12 (rim 6 mm, 4 mm proud of the panel), case (tray + cover) Y 12.1 … 242.15, walls 3, floor 3.5, top 3. Carry/tilt handle pivots on both sides at (Y 40, Z 75); arms and pivot screws add 18 mm per side.
- Front panel: 3.5 mm, face Y −3.5, in three pieces (display section X ≤ 234.5, keypad section X 234.5 … 296, terminal escutcheon X ≥ 296). The escutcheon face is 1.0 mm recessed (Y −2.5). Rear panel 3.5 mm, Y 237 … 240.5.
- **AFE board** 180 × 120: **X 216 … 396, Y 1 … 121**, bottom face at Z = 10. Front holes (4,4), (176,4) on 5 mm F-F standoffs on the bezel, rear holes on tray bosses. UNKNOWN BNCs (Amphenol 031-6575, 1/2-28 UNEF × 8.6 thread from the body face at Y 1): **Lcur X311, Lpot X333, Hpot X355, Hcur X377, Z 19.3** (22 mm pitch, 4TP fixture compatible). Body on a 0.9 mm ring behind the escutcheon, washer + nut on the escutcheon face, 2.2 mm of thread beyond the nut. LED_MEAS (3 mm R/A) at X 366, Z 13.6. Shield can: the ECO-2 outline moved +161 mm in X with the AFE, front fence at Y 17.8 (was 17.0).
- **MAIN board** 150 × 110: **X 246 … 396, Y 126 … 236**, bottom face at Z = 10. Rear connectors (sheet-metal X + 161): USB-C X 261, RJ45 X 286, microSD X 309.3 (USB-C and microSD in 45° pockets, 1.5 mm panel wall). **Rear TRIG BNCs removed**: TRIG harness on J403 (JST PH 4-pin: 1 TRIG_IN, 2 GND, 3 TRIG_OUT, 4 GND). Front-edge connectors J501 (AFE, X ≈ 340), J502 (FRONT, X ≈ 374.5), J503 (display FFC, X ≈ 291). Hole (4,106) bonds to CHASSIS.
- **PSU board** 70 × 110: **X 8 … 78, Y 126 … 236**, bottom face at Z = 10, under a V-0 mains hood. IEC C14 inlet (fuse drawer + switch) on the rear panel at X 35, Z 75. PE/FE stud M4 at X 170, Z 25. Hole (4,106) bonds to PE.
- **FRONT board** Rev B, U-shaped 386 × 125: vertical, component face at **Y 8.3**, **X 8 … 394, Z 5 … 130**, display cutout X 40.5 … 208.4 from Z 25.5 (open top). 9 M3 holes on panel bosses (JSON `front_board.holes_M3`). 38 keys (6 × 6 × 7.3 tactile) at the JSON positions, one keycap colour. EC11E encoder at (362, 98), knob D32. LED_STBY (23, 28) lights the ring around the round power key; LED_RMT (308, 104). Panel-mount TRIG IN (X 311) and TRIG OUT (X 333) BNC jacks (3/8-32) and a 4 mm GND binding post (X 377), all at Z 60, pass through FRONT clearance holes D14/D14/D12.
- **Display** Riverdi RVT70HSBNWN00 (7 in, 1024 × 600, EVE4): module X 42 … 206.9, Z 27 … 127, Y 0 … 10.56, clamped by a printed retainer (4 screws through the FRONT board) against a 2 mm clear lens 164 × 96 in a rear pocket of the panel. Window 156 × 88 centred at (124.45, 77). 20-way 0.5 mm FFC to MAIN J503.
- Grounding: 1.5 mm Al ground plate on the floor, bonded to PE (IEC inlet PE, rear stud, PSU H101, MAIN H301, front GND post).
- Feet: 4 × printed with TPU pads. Handle detents: carry, flat (folded over the top), tilt (about 9°).

6. Power budget

Rail	Source	Load	Current (typ/max)
±15 V raw	RAC20-15DK (±15 V, 0.67 A each)	AFE LDOs	200 / 265 mA (+15 V), 165 / 215 mA (−15 V)
+12VA / −12VA	LT3045 / LT3094 on AFE	12× THS4631 + switches	165 / 215 mA
+5VA	LT3045 on AFE (from +15 V)	ADA4940 ×2, ref, 1.8 V LDO	40 mA
+5V	IRM-20-5	MAIN, display, AFE digital + relays	0.9 / 2.2 A
+3V3 (MAIN)	TPS62130	MCU, PHY, display logic	350 / 700 mA
Display BLVDD	+5V direct	backlight	250 / 400 mA
+3V3D (AFE)	AP2112K-3.3	FPGA IO, DAC DVDD, ADC VIO, I2C	60 mA
+1V2 (AFE)	AP2112K-1.2	FPGA core	10 mA

Total ≈ 10 W typical, 16 W worst case at the mains input (verify/ report, section K).

7. Firmware and software summary

- FPGA (iCE40UP5K, open toolchain yosys + nextpnr-ice40): DDS, DAC interface, dual AD4003 reader, window generator, 4-channel complex MAC, raw-capture RAM, SPI register slave. The bitstream is stored in MCU flash, and the MCU loads it over SPI slave config at every boot. There is no FPGA flash, and field updates ship together with the MCU image.
- MCU firmware (STM32H743, C11, CMake + arm-none-eabi-gcc): measurement engine, auto-ranging, correction and calibration math, SCPI parser (IEEE 488.2 + E4980A-style subset), EVE UI, USB-TMC (TinyUSB), LAN (lwIP raw TCP 5025), FatFs on SD.
- Host software (Python 3.10+): `za1` package with a SCPI driver (VISA/USB-TMC or raw socket) and a PySide6/pyqtgraph GUI (sweeps, Bode/Nyquist, equivalent-circuit fitting, CSV export). It includes an instrument simulator for offline use and CI.

See 02_Interface_Control.pdf for register maps, pin maps and SCPI.