ZA-1 Theory of Operation

Document ZA1-TOO-003 Rev A

1. Measurement principle: auto-balancing bridge

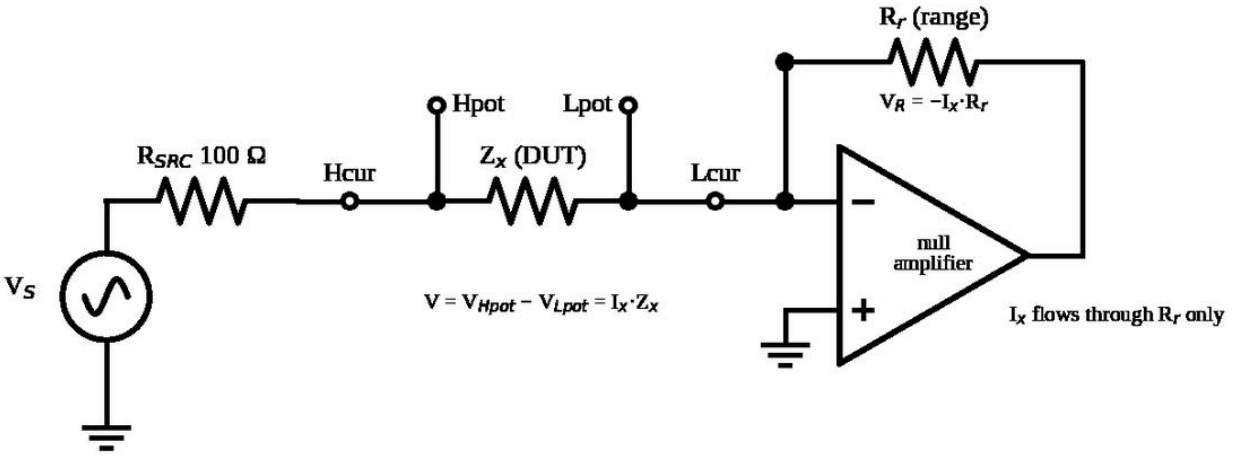


Figure 1. Simplified auto-balancing bridge. The null amplifier holds the Lpot terminal at 0 V, so all of the current through the part under test flows through the range resistor Rr, where it is measured.

The null amplifier forces the Lpot node to 0 V. All DUT current I_x then flows through the range resistor Rr, and none flows through the stray capacitance of the Lpot/Lcur cables. The instrument measures two voltages:

- **V** = V(Hpot) − V(Lpot) = I_x · Z_x (measured with a difference amplifier, so a small Lpot residual cancels)
- **V_R** = V(ISNS_TOP) − V(LCUR_S) = −I_x · Rr (measured Kelvin across Rr, so relay contact resistance is excluded)

Both Kelvin taps of Rr are read through unity-gain FET buffers (ECO-5), exactly like Hpot and Lpot, so the difference amplifier's 1 kΩ input resistors never load the range resistor. With the range capacitor Cc across Rr, the nominal feedback impedance is Z_f = Rr ∥ Cc, and **Z_x = −Z_f · V / V_R**. Both voltages go through identical gain chains (buffer → difference amplifier → PGA ×1/×10/×100 → ADA4940 driver), and are digitised **simultaneously** by two AD4003 ADCs that share one CNV edge and one reference. In the ratio, the ADC reference value, its noise, the window scaling and the source amplitude all cancel. What is left is the ratio of the two analog path gains, which factory calibration measures as a complex correction K(range, gains, f).

2. Signal source

The FPGA runs a 32-bit NCO at 24 MSPS (a 48 MHz clock divided by 2). A 1024-entry quarter-wave ROM gives a 16-bit sine. Firmware scales it with AMPL, adds DAC_OFS and sends it to the AD9744 (14-bit). Frequency resolution is 24e6/2^32 = 5.6 mHz. Optional LFSR phase dither spreads the phase-truncation spurs, which could otherwise alias onto f for some "round" tuning words. The analog chain after the DAC is:

1. Differential current output into 2×49.9 Ω gives ±1 V. A 470 pF differential capacitor adds a first pole at 3.4 MHz.

2. A THS4631 difference amplifier converts to single-ended (gain 1).
3. A 2 MHz unity-gain Sallen-Key Butterworth filter follows. The first DAC image at 23 MHz is attenuated by the combined poles (≈ 60 dB) and the DAC sinc response (≈ 28 dB).
4. The attenuator has two relay-switched −20 dB dividers, K5 and K6: 909/100 Ω, then 9.09 k/1.00 k. Attenuating in the analog domain keeps the DAC near full scale at low test levels, so SNR stays high. Nominal ratios are about 0.099 and 0.098. Exact values come from level calibration.
5. The THS4631 driver (gain 2.8) produces 1.98 Vrms open-circuit at full scale.
6. K7 connects the source to Hcur through R_SRC = 100 Ω. When released, it discharges the DUT through 570 Ω.

The level at the DUT is not controlled open-loop. The **V channel measures it directly**, and in ALC mode the firmware servos AMPL until V matches the setpoint.

3. Current path and range resistors

Range	Rr	Cc (ECO-5)	Full-scale |Z| at PGA ×1	Max f
0	100 Ω	470 pF	~10 Ω … 300 Ω	1 MHz
1	1.00 kΩ	220 pF	300 Ω … 3 kΩ	1 MHz
2	10.0 kΩ	220 pF	3 kΩ … 30 kΩ	500 kHz
3	100 kΩ	220 pF	> 30 kΩ	100 kHz

Auto-ranging uses VPEAK and IPEAK. It picks Rr and the two PGA gains so that both ADCs sit at 20–80 % of full scale. Very low impedance uses Rr = 100 Ω with V-gain ×10/×100; very high impedance uses Rr = 100 kΩ with I-gain ×10/×100. Range changes are make-before-break, so the null-amp loop is never open.

3.1 Null-loop compensation (ECO-5, set by simulation)

The null loop runs through the four test cables, which are transmission lines with resonances between about 10 MHz (4 m) and 50 MHz (1 m). The loop is therefore shaped so that it has no gain left at those frequencies:

- LPOT_IN reaches the null amplifier through **1.00 kΩ**, and a **15 pF** capacitor from the amplifier output (TIA_AMP) to its input closes a local loop. Above ~10 MHz the amplifier follows this local loop instead of the cable loop.
- A **47 Ω** resistor (TIA_AMP → TIA_OUT) isolates the amplifier from the relay, Cc and cable capacitance.
- **Cc = 470 pF / 220 pF** across Rr sets the high-frequency feedback factor, independent of cable length.
- **49.9 Ω + 1 nF** RC terminations on LPOT_IN and on the Lcur BNC damp the cable resonances.
- The Lpot buffer reads LPOT_IN through its own 100 Ω + clamp, not the amplifier's summing node.

Simulated on the real netlist (4 ranges × 0/0.5/1/2/4 m cables × 11 DUTs): bridge-loop phase margin ≥ 49° with cables up to 2 m and ≥ 39° at 4 m; peak sensitivity ≤ 2.7 dB (≤ 2 m). The price is a smaller balance gain at the top of the band (|T| ≈ 1–4 at 1 MHz). The resulting error is linear and is removed by factory calibration and the user's OPEN/SHORT/LOAD correction (see verify/ report). The firmware uses Z_f = Rr ‖ Cc as the nominal range impedance, so the factory K table only carries small residuals.

3.2 Input protection (ECO-5)

A charged capacitor connected to UNKNOWN is the most common way LCR meters are damaged. The Hcur clamp diodes sit behind the 100 Ω source resistor (anti-surge thick film), the Lcur clamp behind a 22 Ω anti-surge resistor, and Hpot/Lpot behind 100 Ω / 1 kΩ. A 100 µF capacitor charged to 50 V (125 mJ) drives at most ≈ 0.2 A into the BAV199 clamps (rating 1 A for 1 ms). Always discharge capacitors before connecting them; see the user manual.

4. Sampling and demodulation

- fs = 48 MHz / ADC_DIV, with ADC_DIV ≥ 56 (≤ 857 kSPS).
- **f < fs/2:** sampled normally. **f > fs/2 (≈ 430 kHz – 1 MHz):** coherent **bandpass undersampling**. This is valid because the AD4003 has a 10 MHz input bandwidth and the V and I paths are identical, so aliasing affects both channels the same way. The firmware frequency planner chooses ADC_DIV so the alias sits near fs/4, well away from DC and Nyquist.
- The FPGA multiplies each sample by a 4-term Blackman-Harris window and by cos/sin of the **exact DDS phase at the CNV instant**. It accumulates 64-bit I/Q sums for V and I. The window's −92 dB side-lobes stop the negative-frequency image and harmonics from biasing the fundamental, whether or not the record holds an integer number of cycles. The window gain cancels in the ratio.
- The record is at least 8 signal cycles. The aperture (SHORT/MED/LONG) sets the number of samples. At 1 kHz, MED is about 64 ms.

5. Correction chain (firmware)

1. Raw ratio: H = (V_RE + jV_IM)/(I_RE + jI_IM)
2. Z_raw = −Z_f(range, f) · (G_I/G_V) · H, with Z_f = Rr ‖ Cc (ECO-5)
3. Factory correction: Z_f = Z_raw · K(range, gV, gI, f). K is interpolated in log f (magnitude and phase) from 48 EEPROM points, with a temperature coefficient taken from TMP117 and the stored tempco of Rr.
4. User OPEN/SHORT/LOAD (standard three-term correction): Z_dut = Z_std · (Z_o − Z_sm)(Z_xm − Z_s) / ((Z_sm − Z_s)(Z_o − Z_xm)) for LOAD; OPEN/SHORT only is the special case.
5. Parameter conversion (Cp, Cs, Lp, Ls, D, Q, G, B, Rs, Rp, X, |Y|, θ).

6. Digital architecture

- **FPGA (iCE40UP5K):** DDS, DAC interface, dual AD4003 reader, window generator, complex MAC and raw capture (SPRAM, 16 k pairs). It has an SPI register slave. The bitstream (104 kB) lives in MCU flash, and the MCU loads it in SPI-slave mode at every boot.
- **MCU (STM32H743, 480 MHz):** measurement engine, ranging, calibration, SCPI (USB-TMC, LAN 5025, UART), EVE4 display UI, keypad and encoder, SD card, trigger I/O.
- **Display:** BT817Q EVE4 over QSPI. The MCU sends display lists, not pixels, so the 7" 1024×600 UI needs no MCU frame buffer.

7. Power architecture

Mains goes through an IEC inlet with fuse and switch to the PSU board. There, an EMI filter (X2 capacitors, 2×10 mH common-mode choke, MOV) feeds two **pre-certified** AC/DC modules: RECOM RAC20-15DK (±15 V, isolated, for analog) and MEAN WELL IRM-20-5 (5 V, for digital). Fusing: 2 × T2 A in the inlet drawer, T3.15 A on the PSU board (ECO-5). On the AFE, LT3045/LT3094 LDOs (0.8 µVrms noise, 79 dB PSRR at 1 MHz) produce ±12VA and +5VA. AP2112 LDOs produce the 3.3 V/1.8 V/1.2 V logic and ADC rails. On MAIN, a TPS62130 buck makes 3.3 V. All grounds are common, with the star point at the PSU output connectors. The AFE ground reaches the chassis only through the BNC shells at the front panel.